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(54) Automatic gain control devices

(57) An automatic gain control device with analog to digital conversion comprises a coarse gain control element 14 for an input analog signal, an analog to digital converter (ADC) 16 and a fine gain control element 17 connected to the output of the ADC. A first means 18 is provided for deriving a signl V which is an estimate of the signal level at the output of the ADC, a second means 18, 19 or 18' is provided for deriving a signal V' which is an estimate of the signal level at the output of the fine gain control circuit, and means 20 is provided for deriving an error signal E related to the difference between a desired signal level and V'. A processor 15 is responsive to the signals V and E for performing an iterative control process which adjusts 14 and 17 so that their respective gains and outputs tend to lie within defined limits. The device may be used in a modem.

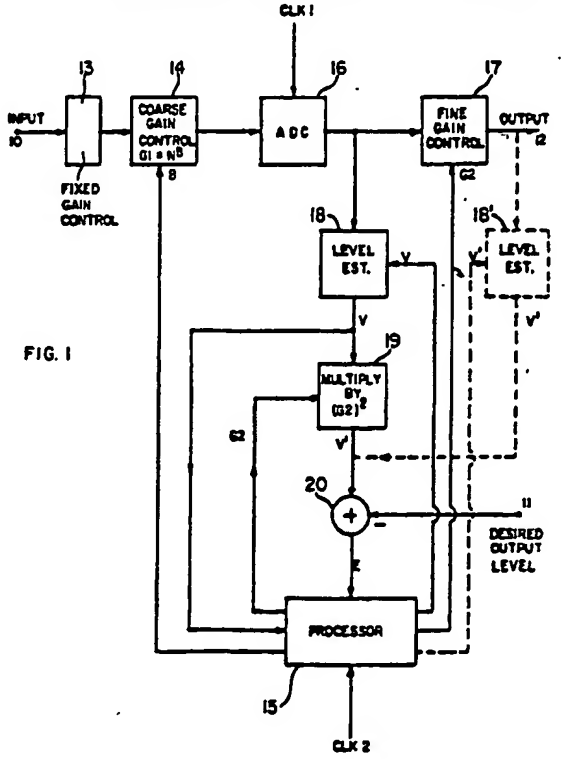

FIG. 1

GB 2 229 333 A

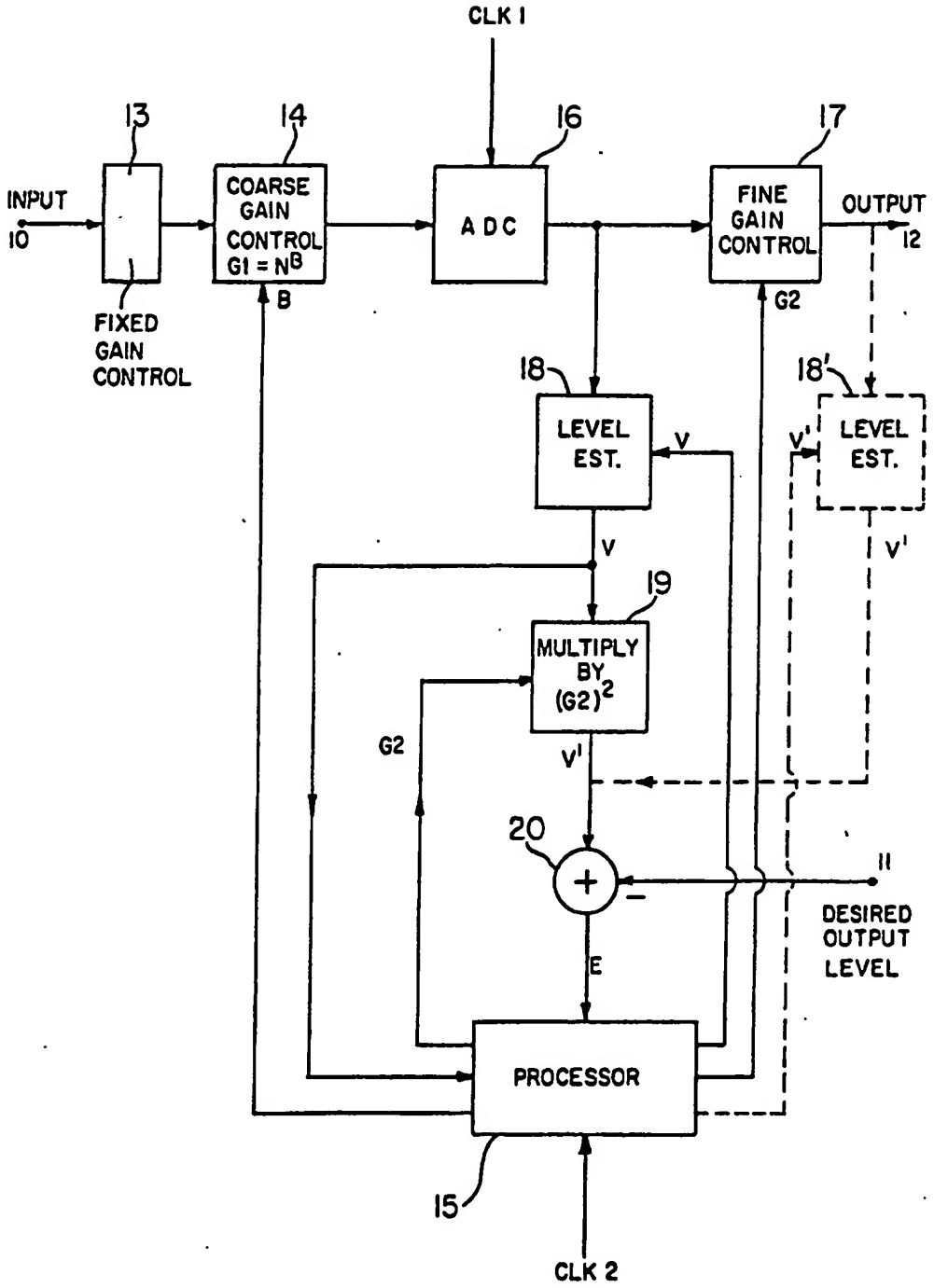
CLK 1
13
14
16
17
INPUT
10
COARSE GAIN CONTROL G1 = N^B
A D C
FINE GAIN CONTROL
OUTPUT
12
B
G2
FIXED GAIN CONTROL
18
18'
LEVEL EST.
V
V'
LEVEL EST.
V
V'
19
MULTIPLY BY (G2)^2
G2
V'
20
11
DESIRED OUTPUT LEVEL
E
PROCESSOR
15
CLK 2

FIG. 1

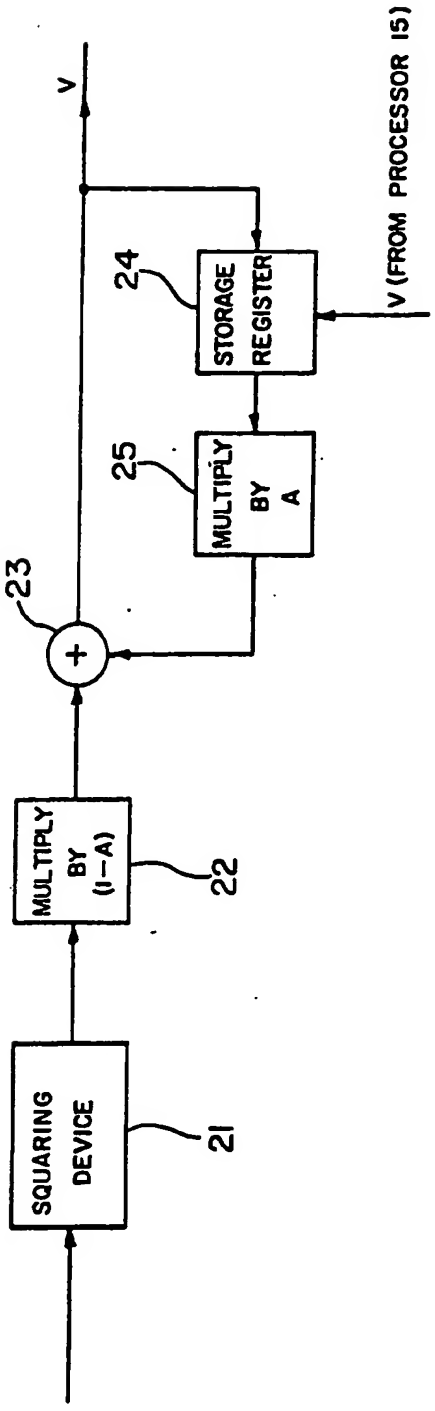
V
V (FROM PROCESSOR 15)
24
STORAGE REGISTER
25
MULTIPLY BY A
23
+
MULTIPLY BY (1-A)
22
SQUARING DEVICE
21

FIG. 2.

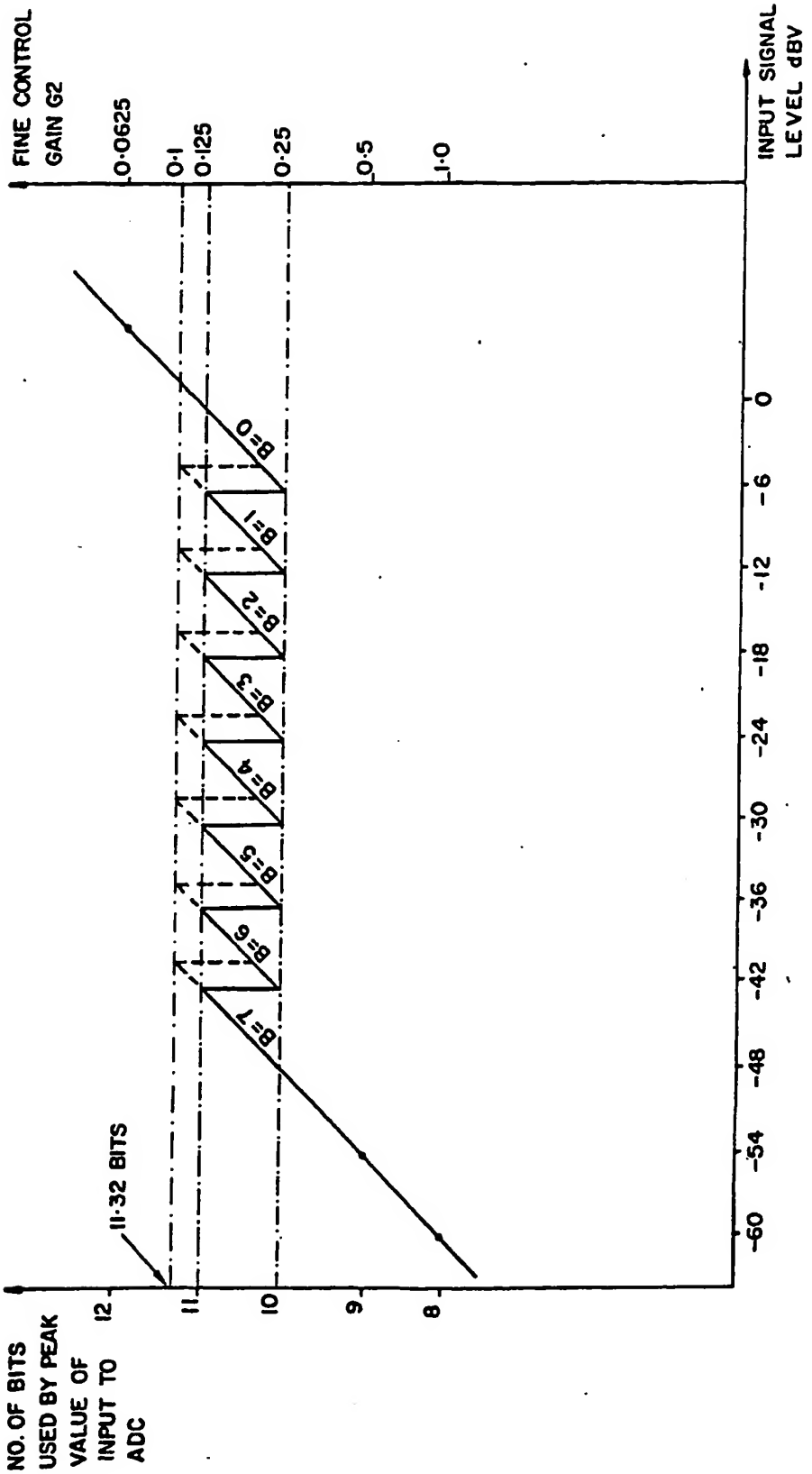
FINE CONTROL
GAIN G2
0·0625
0·1
0·125
0·25
0·5
1·0
INPUT SIGNAL
LEVEL dBV
0
-6
-12
-18
-24
-30
-36
-42
-48
-54
-60
B=0
B=1
B=2
B=3
B=4
B=5
B=6
B=7
11·32 BITS
NO. OF BITS
USED BY PEAK
VALUE OF
INPUT TO
ADC
12
11
10
9
8

FIG. 3

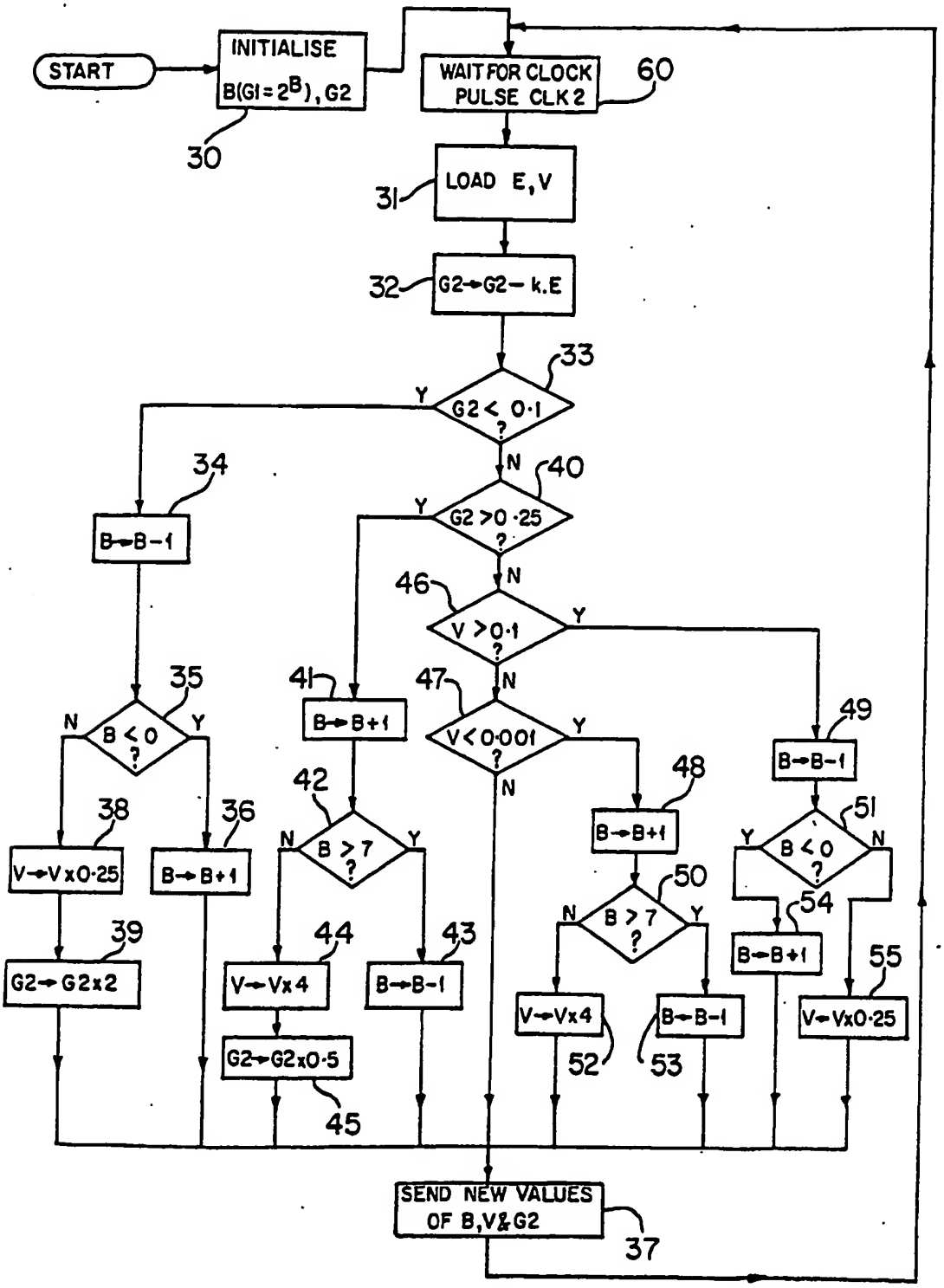
START
INITIALISE B(GI=2^B), G2
30
WAIT FOR CLOCK PULSE CLK2
60
31
LOAD E,V
32
G2→G2−k.E
33
G2<0·1 ?
Y
N
34
B→B−1
40
G2>0·25 ?
Y
N
46
V>0·1 ?
Y
N
35
B<0 ?
N
Y
41
B→B+1
47
V<0·001 ?
Y
N
49
B→B−1
38
V→Vx0·25
36
B→B+1
42
B>7 ?
N
Y
48
B→B+1
51
B<0 ?
Y
N
50
B>7 ?
N
Y
54
B→B+1
39
G2→G2x2
44
V→Vx4
43
B→B−1
V→Vx4
52
B→B−1
53
55
V→Vx0·25
G2→G2x0·5
45
SEND NEW VALUES OF B,V&G2
37

FIG. 4

AUTOMATIC GAIN CONTROL DEVICES

This invention relates to an automatic gain control device with analog to digital conversion, and is concerned with the situation where an analog signal of unknown and perhaps varying level is required to be converted into a digital signal with a constant predetermined level. In this specification , as will be understood by those skilled in the art, the term "level" means a signal statistic such as, but not limited to, mean square value or mean rectified value.

The invention has particular but not exclusive application to the reception of multilevel data by modems.

In many communication systems the level of the signal is unknown prior to its reception and so the receiver cannot be preconditioned to suit the received signal. It is a property of many receivers that they require the level of a signal to lie between narrow limits for successful operation of the receiver hence, before being passed to the main part of the receiver, the signal level is adjusted by a special device known as an automatic gain control (AGC).

This device is especially required when the receiver consists of digital circuitry being used to process an analog communications signal because in this instance the signal must pass through an analog to digital converter (ADC). The ADC introduces noise which is essentially independent of the signal level and so to keep the signal to noise ratio (S/N) at acceptable levels an AGC is required. If the signal level is too low the signal to noise ratio will be unacceptably low

and if the signal level is too high the ADC will saturate thus grossly distorting the signal. However as far as the ADC is concerned the limits between which the signal must be maintained can be defined, and these limits are usually not very severe. The signal is usually required to be held to much more rigid levels for the remainder of the receiver.

In some communications systems for example AM and FM radio transmissions, a carrier signal is present and so the receiving apparatus can base the operation of its AGC on this component of the signal. In other systems for example those using single sideband or quadrature amplitude modulated signals the carrier is suppressed and so the information necessary for controlling the AGC must be derived from the information bearing part of the signal. It is mainly to this class of signal (suppressed carrier) that this invention applies. Situations where the invention will prove particularly useful are the reception of radio signals over transmission paths of unknown and/or varying attenuation and the reception of data signals transmitted on switched or leased telephone circuits. The problem is particularly acute when multilevel data is being transmitted over the channel, as decisions have to be made based on the actual level of the signal at certain instants relative to its average power level.

It is therefore an object of the invention to provide an AGC providing rapid initial level adjustment of a signal of unknown amplitude and the subsequent tracking of that signal. Further, during this tracking period the proposed device should rapidly adapt to any sudden and gross changes in signal level while being able to follow slower changes with minimum deleterious effects.

Accordingly, the present invention provides an automatic gain control device with analog to digital conversion, comprising:

first means providing a coarse gain control element for an input analog signal and whose gain G1 can be multiplied by a constant factor N or its inverse 1/N to vary G1 between predetermined limits,

second means providing an analog to digital converter (ADC) connected to the coarse gain control element for converting the analog signal from the coarse gain control element into digital form,

third means providing a fine gain control element connected to the output of the ADC and having a variable gain G2,

first estimating means for deriving a signal V which is an estimate of the signal level at the output of the ADC,

second estimating means for deriving a signal V' which is an estimate of the signal level at the output of the fine gain control element,

fourth means for deriving an error signal E related to the difference between a desired signal level and the estimate V' of the signal level at the output of the fine gain control element, and

fifth means responsive to the signals V and E for performing an iterative control process which adjusts G1 in an attempt to bring V within predetermined upper and lower limits and adjusts G2 to make V' tend towards the desired signal level,

wherein in such control process when G1 is adjusted a compensating adjustment is made to G2 to maintain the product of G1 and G2 constant, except that when G2 lies within predetermined upper and lower limits whose ratio is at least equal to the factor N and V lies outside its predetermined limits an adjustment is made to G1 in an attempt to bring V within or closer to its predetermined limits without any compensating adjustment to G2.

Preferably, the ratio of the predetermined upper and lower limits for G2 is slightly greater than the factor N.

Further, the first estimating means preferably comprises means for performing a memoryless non-linear operation followed by a low pass digital filter, and wherein following multiplication of the gain G1 by N or 1/N the control process multiplies the signal value(s) stored in the signal memory of the filter by an amount which changes the stored signal value(s) to those which would have arisen if the first estimating means had been operating on the modified signal at the output of the ADC for a time much greater than the time constant of the filter.

Naturally, the various means specified above need not be implemented as separate elements or components of the device.

The advantage of the invention is that the combination of a coarse gain control element and a fine gain control element together with a novel control strategy enables an effective and fast acting automatic gain control device to be implemented.

Furthermore, the invention can be implemented in a simple manner in which the only digital arithmetic operations required to be performed are addition, subtraction and multiplication which are relatively simple and cheap to implement, thus avoiding the need for more complex operations such as division or square roots.

An embodiment of the invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a block circuit diagram of an embodiment of an AGC device according to the invention,

Figure 2 illustrates the signal level estimator of figure 1,

Figure 3 is a graph illustrating the operating characteristics of the circuit of figure 1, and

Figure 4 is a flow diagram of the operation of the AGC device of figure 1.

A general description of the embodiment and its operation will first be given with reference to figure 1, followed by a more detailed description referring also to figure 2 to 4.

There are two inputs to the device of figure 1, one input 10 for the analog signal whose level is to be controlled and the second input 11 for the desired signal level. There is one output from the device, namely the output 12 for the digital signal with a controlled level.

Ignoring for the moment the fixed gain control element 13, in the embodiment the analog signal is first passed through a coarse gain control element 14 which can apply coarse level changes to the signal. The gain G1 of this element 14 can be multiplied by a constant factor N or its inverse 1/N in response to a first control signal B to vary G1 between predetermined limits. The signal B is a binary number which is supplied by a digital microprocessor 15 and which defines the gain as G1 = N**B (N to the power B). The constant factor N would typically be two although other values may be used. It will be clear that an increase in the value of B by one effects multiplication of the current gain G1 by N, whereas a decrease in the value of B by one effects multiplication of the current value of G1 by 1/N.

The coarse gain control element can be implemented by appropriate use of a multiplying D\A converter (digitally controlled analog amplifier) together with some fixed gain amplifier or attenuator. As mentioned, the exact gain selected at any instance is under the control of the processor 15.

After passing through the coarse gain control element 14 the signal is next passed through a 12-bit analog to digital converter (ADC) 16 and then through a fine gain control element 17 capable of applying fine level changes to the signal. The fine gain control element 17 may be a digital multiplier. The gain G2 of the element 17 is directly defined by a binary number supplied by the processor 15.

The level of the signal at the output of the ADC is estimated by feeding into a signal level estimator 18 which gives a digital output signal V representing the estimate. This value V is supplied to the processor 15

as shown. Further, for a reason which will be described later, the processor 15 can supply a processor-generated value of V to the estimator 18 to replace the estimated value.

The signal level at the output of the fine gain control element 17 is also estimated, and this is achieved by multiplying the output V of the estimator 18 by the square of G2 in the element 19 to provide the required level estimate V'.

An error signal E is then derived in the element 20, this being the difference between the estimated level V' of the output from the fine gain control element 17 and the desired signal level supplied at input 11.

At this point it should be understood that the level V' of the signal at the output of the fine gain control element 17 can alternatively be estimated by omitting the squaring element 19 and any other connection from estimator 18 to element 20, and providing a second signal level estimator 18' connected to the output of the fine gain control element 17 and to the input to the element 20 as shown in dashed lines. Similar to the case of the estimator 18, the processor 15 can supply a processor-generated value of V' to the estimator 18' to replace the estimated value. For the moment, however, it will be assumed that the squaring element 19 is used to generate V'.

The digital processor 15 takes as its input the error signal E. Using this error signal the gain G2 of the fine gain control element 17 is adjusted by an amount proportional to the error signal E and in a direction to reduce the error. This done repeatedly would lead to an implementation of an AGC, but without

the control strategy outlined below would lead to unacceptably slow convergence under many typical operating conditions.

The control strategy is implemented by the digital processor 15. The processor by following the logic of a decision tree may make a further adjustment to the fine gain control element 17 together with a compensating adjustment to the coarse gain control element 14. Alternatively an adjustment may be made to the coarse gain control element alone. In essence, the processor 15 determines if the gain G2 of the fine gain control element 17 has been brought outside predetermined limits by its first adjustment. If it has then it is adjusted so as to either lie once again between these limits or to be closer to these limits by multiplying it by N or 1/N as appropriate, provided that the gain G1 of the coarse gain control element 14 can be multiplied by the inverse of that number and still remain within its allowed limits as determined by the range of the exponent B.

If the gain G2 of the fine gain control element 17 lies between its allowed limits and the estimated level V of the output signal from the ADC 16 lies outside predetermined limits then a further adjustment is made to the coarse gain control element 14, if this is possible, without any compensating adjustment to the fine gain control element 17.

All adjustments are automatic and are made in such a direction so that the error will be reduced. Hysteresis may be included in the adjustment strategy for the coarse gain control element 14 to prevent limit cycles occurring due to non-linearities in the ADC. The entire strategy is repeated frequently at least until the error signal E is reduced to acceptable limits.

A suitable repetition frequency would be equal to the sample frequency of the ADC 16 or submultiple of the sample frequency. In figure 1 the sample frequency is indicated as CLK1 input to the ADC and may be derived from the incoming signal. The rest of the device repeats at this frequency or a submultiple thereof, indicated for simplicity by the CLK2 input to the processor 15.

Even after the error has been brought to lie within acceptable limits the control and adjustment strategy may be continued so that any subsequent drifting or sudden changes in signal level can be dealt with.

The level estimator 18 consists of a device for performing a memoryless non-linear operation such as a numerical squaring or magnitude extracting (rectifying) device followed by a lowpass digital filter. The signal memory of the filter should be adjustable in response to a processor-generated value for V to compensate immediately for any gross changes in signal level resulting from adjustments to the coarse gain control circuit 14, as to be described.

Typical values relating to the foregoing are as follows. The nominal maximum level of the input signal is 0 dBV. The peak to root mean square (RMS) value is 4.0. The ADC 16 is a 12-bit device with an input range of -1.0 to +1.0 volts. The desired RMS value of the digital output from the automatic gain control device is 0.015625. The precision afforded the peak value of the signal is to be at least 10 bits over a large range of input signal levels. The coarse gain control is an analog amplifier with a digitally controlled gain. The gain is N**B (N to the power of B) where in this example N is two and B is an integer in the range from 0 to 7,

providing 8 values of gain. The value of B is supplied to the coarse gain control element 14 by the processor 15 for control purposes. In order to reconcile the nominal maximum value of the input signal with the range of the ADC 16 a fixed voltage gain of 0.125 is provided before the input to the coarse gain control element 14 by the fixed gain element 13.

The signal level estimator 18 is shown in Fig.2. In this case it consists of a numerical squaring device 21 followed by a first order recursive low pass filter comprising the elements 22 to 25. The value of A is an appropriately chosen constant being close to but less than one. The storage register (signal memory) 24 of the low pass filter normally contains the previous output V from the filter but this value can be overwritten with a new value of V produced by the processor 15. This is because the low pass filter has an unacceptable transit time after coarse gain adjustment in element 14. Thus each time the gain G1 is multiplied by 2 or 0.5 the processor 15 takes the existing value of V at the filter and multiplies it by 4 or 0.25 respectively and replaces the value V in the register 24 with the processor-generated value.

It will be understood by those skilled in the art that the digital low pass filter may have more than one register such as the register 24 for storing signals internal to the filter. In such case the signal in each such register will be multiplied as described above for the register 24.

Since the level estimator 18 provides an estimate V of the signal level at the output from the ADC as a mean square value, the estimate V' of the output level from the fine gain control circuit obtained by multiplying V by G2 squared is also a mean square value. Thus this is

compared in element 20 with the desired mean square value supplied at input 11, ie 0.015625 squared, to produce the error signal E.

The fine gain control element 17 processes the signal from the ADC 16 at a rate equal to the sampling rate of the ADC, ie at the rate CLK1. The rest of the device, namely the level estimator 18, the scaling by G2**2 (G2 to the power of 2) in element 19 and the the error calculation in element 20 may, as previously described, operate at a repetition rate (CLK2) which may be equal to CLK1 or a submultiple thereof. Suitable control signals are issued by the processor 15 at this rate.

Fig. 3 shows the values to which B (and hence also G1) and G2 will tend to converge as functions of the input signal level. The horizontal axis shows the level of the input to the fixed analog gain circuit in dBV. There are two vertical scales, the one on the left shows the number of bits occupied by the peak value of the signal after analog to digital conversion. The other shows the value of G2. The solid line shows permitted steady state values for G2 and B. The value of B is constant between discontinuities on the line. The dashed curve shows additional allowed values for G2 which are used to implement hysteresis.

Hysteresis is used to prevent any nonlinearity present in the ADC 16 from causing limit cycle behaviour in the control procedures. Hysteresis is achieved by making the ratio of the upper permissible value of G2 to the lower value of G2 slightly greater than the mantissa N of the gain G1 of the coarse gain control element 14. In this example N is two and the the nominal range of G2 is from 0.125 to 0.25. Hysteresis is implemented by

extending this range at its lower end so that G2 may vary between 0.1 and 0.25. The extension could also be applied at the upper end of the range or at both ends.

G2 is also allowed to depart from its nominal range when B is at one of its two limiting values. This is apparent in Fig. 3 for values of input signal level below -48 dBV and above 0 dBV. The reason why G2 must lie outside its limits in these circumstances is that there does not exist a permissible value for B which will keep G2 within its limits and also allow the output signal from the fine gain control to have the correct level. By permitting G2 to increase above 0.25 for input signals with a level below -48 dBV the output level can still be maintained at the correct value but precision is lost in the ADC. If the input signal level should be above 1.94 dBV (approximately) than the minimum value of B (hence of G1) has been reached, hence the correct overall gain can only be maintained by permitting the value of G2 to go below 0.1. Occasional saturation of the ADC will begin to occur when the value of G2 drops below 0.0625.

In this embodiment the processor 15 is programmed to implement the flow diagram shown in figure 4. This assumes that the signal V' is derived from the element 19 (ie the level estimator 18' is not present) and that the signal level estimator 18 includes a squaring device 21 rather than a magnitude extractor (the changes consequent on the latter will be dealt with later) or other memoryless non-linear operating device.

First it should be pointed out that the processor has three inputs, namely the output from the level estimator V, the error signal E and the clock CLK2 which may be equal to CLK1, and provides three outputs:

(i) a digital number B this being the exponent of the value of gain to be used by the coarse gain control until another value of B is provided,

(ii) the digital number G2, this being the value of gain to be used by the fine gain control circuit until another value of G2 is provided, and

(iii) when appropriate the new value for V which overwrites the value of V currently in the storage register of the digital filter.

Referring to the flow diagram, B and G2 are first initialised at 30 to suit the expected input signal level. Upon receipt of a clock pulse CLK2 at step 60 the latest values of E and V are loaded at 31 into storage registers accessible by the processor 15. The next step 32 is that an adjustment is made to the value of G2 stored in the processor registers. The adjustment is proportional to minus the value of the error E, the constant of proportionality k being an appropriately chosen constant.

At step 33 G2 is tested to see if it lies below its allowed range. If so, B is decremented by 1 in step 34 and then B is tested in step 35 to see if it has been brought below its lower limit. If it has, B is increased by 1 at step 36 and control passes to step 37 to be described later. If it hasn't, V is multiplied by 0.25 at step 38 for providing a processor-generated value of V to replace the value currently stored in the estimator 18, for the purpose previously described. It is pointed out at this stage that the value of V stored in the estimator 18 which is replaced by the processor-generated value will be the "true" estimate as derived from the output of the ADC 16 unless on the

previous iteration through the flow diagram the processor also generated a value for V at step 38 or at any of the other steps to be described which involve multiplication of V, namely steps 44, 52 and 55.

Next, at step 39, G2 is multiplied by 2 to compensate for the halving of G1 which will be brought about by the decremented value of B resulting from step 34. Again, control now passes to step 37.

If at step 33 G2 does not lie below its allowed range, it is tested in step 40 to see if it lies above its allowed range. If it does, B is incremented by 1 (step 41) and then tested for being above its upper limit (step 42). If it is, B is decreased by 1 at step 43 and control passes to step 37. If it isn't, V is multiplied by 4 at step 44 for providing a processor-generated value of V to replace the value currently stored in the estimator 18.

Next, at step 45, G2 is multiplied by 0.5 to compensate for the doubling of G1 which will be brought about by the incremented value of B resulting from step 41. Control now passes to step 37.

If G2 is found to lie between its limits then two tests (steps 46 and 47) are carried out to see if V lies between suitably chosen limits, and if it does control passes to step 37.

If V lies outside these limits then B is adjusted as appropriate (steps 48 and 49) without a corresponding adjustment being made to G2. This is necessary because it is the nature of the update to G2 that the value of G2 may move slowly under certain conditions despite the overall gain (G1 multiplied by G2 multiplied by fixed analog gain) being grossly incorrect.

Following adjustment of B at step 48 or 49, tests (steps 50 and 51) and actions (steps 52 to 55) the same as those previously described are carried out, and control passes to step 37.

The actions resulting from the testing of V implement a form of autorangeing. Typical limits for V for this test would be about 6dBV above its normal upper limit and about 6dBV below its normal lower limit. In this example the normal upper limit for V occurs when G2 has settled at a value of 0.1 and this value of V is equal to 0.025 (approx) and the normal lower limit for V occurs when G2 has settled at a value of 0.25 and this value of V is equal to 0.004 (approx). Thus autorangeing might typically take place when V lies outside the range 0.001 to 0.1.

At step 37, via whichever route it is reached, the new values of B, G2 and V (any or all of which may be the same as the previous values) are issued as control signals to the coarse gain control element 14, the fine gain control element 17 and the digital filter respectively.

The processor 15 then waits at step 60 for a clock pulse CLK2 which causes a repetition of the entire operation, apart from the initialisation, to begin.

The foregoing assumes that the processor continues to cycle round the loop indefinitely while the AGC is on, irrespective of whether the error E has been brought within acceptable limits. This is preferable, but not essential. If it is desired to terminate operations when E has been brought within acceptable limits, this is simply achieved by adding a test between steps 31 and 32. The test would simply consist of determining

whether E lay between predetermined upper and lower limits for at least one and preferably a predetermined number (say 100) CLK2 signals.

As mentioned above, the flow diagram is based upon the assumption that that the signal level estimator 18 includes a squaring device 21 rather than a magnitude extractor before the low pass filter. If a magnitude extractor is used, the only changes to the flow diagram are that in steps 38 and 55 the value V is multiplied by 0.5 rather than 0.25, and in steps 44 and 52 the value V is multiplied by 2 rather than 4. Also, the input at 11 would be the desired mean rectified value of the output signal at 12.

Further, if the output signal level estimate V' is derived using a second estimator 18' as shown in dashed lines in figure 1, steps 38, 44, 52 and 55 of the flow diagram would be followed by eqivalent operations on V', and step 37 would also send the new value of V' to the signal memory of the estimator 18'.

Finally, it is to be pointed out that although figure 1 has shown elements 17 to 20 as separate from the microprocessor 15, it will be clearly understood that any or all of these elements could be implemented by the microprocessor and its storage. On the other hand, not only could these elements be separate hardware elements, but the processor 15 itself could be replaced by suitably designed logic which would implement the flow diagram of figure 4.

CLAIMS:

1. An automatic gain control device with analog to digital conversion, comprising:

first means providing a coarse gain control element for an input analog signal and whose gain G1 can be multiplied by a constant factor N or its inverse 1/N to vary G1 between predetermined limits,

second means providing an analog to digital converter (ADC) connected to the coarse gain control element for converting the analog signal from the coarse gain control element into digital form,

third means providing a fine gain control element connected to the output of the ADC and having a variable gain G2,

first estimating means for deriving a signal V which is an estimate of the signal level at the output of the ADC,

second estimating means for deriving a signal V' which is an estimate of the signal level at the output of the fine gain control element,

fourth means for deriving an error signal E related to the difference between a desired signal level and the estimate V' of the signal level at the output of the fine gain control element, and

fifth means responsive to the signals V and E for performing an iterative control process which adjusts G1

in an attempt to bring V within predetermined upper and lower limits and adjusts G2 to make V' tend towards the desired signal level,

wherein in such control process when G1 is adjusted a compensating adjustment is made to G2 to maintain the product of G1 and G2 constant, except that when G2 lies within predetermined upper and lower limits whose ratio is at least equal to the factor N and V lies outside its predetermined limits an adjustment is made to G1 in an attempt to bring V within or closer to its predetermined limits without any compensating adjustment to G2.

2. An automatic gain control device as claimed in claim 1, wherein the ratio of the predetermined upper and lower limits for G2 is slightly greater than the factor N.

3. An automatic gain control device as claimed in claim 1 or 2, wherein the first estimating means comprises means for performing a memoryless non-linear operation followed by a low pass digital filter, and wherein following multiplication of the gain G1 by N or 1/N the control process multiplies the signal value(s) stored in the signal memory of the filter by an amount which changes the stored signal value(s) to those which would have arisen if the first estimating means had been operating on the modified signal at the output of the ADC for a time much greater than the time constant of the filter.

4. An automatic gain control device as claimed in claim 3, wherein the first estimating means comprises a squaring device followed by a low pass digital filter, and wherein following multiplication of the gain G1 by N

or 1/N the control process multiplies the signal value(s) stored in the signal memory of the filter by N squared or the inverse of N squared respectively.

5. An automatic gain control device as claimed in claim 3, wherein the first estimating means comprises a numerical rectification device followed by a low pass digital filter, and wherein following multiplication of the gain G1 by N or 1/N the control process multiplies the signal value(s) stored in the signal memory of the filter by N or the inverse of N respectively.

6. An automatic gain control device as claimed in any preceding claim, wherein some or all of the third to fifth means and the first and second estimating means are implemented by a programmed microprocessor.

7. An automatic gain control device with analogue to digital conversion substantially as herein described with reference to and as illustrated in the accompanying drawings.

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